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Solution-Processable Low-Voltage and Flexible Floating-Gate Memories Based on an n-Type Polymer Semiconductor and High-*k* Polymer Gate Dielectrics

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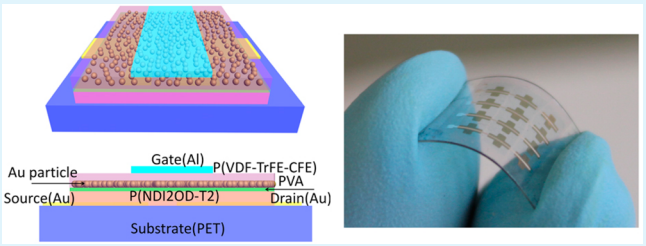
Supporting Information

ABSTRACT: High-performance low-voltage flash memories based on organic floating-gate field-effect transistors are prepared by a solution process for the first time. Transistors with a high-mobility n-type polymer semiconductor, poly-{[*N*,*N*′-bis(2-octyldodecyl)naphthalene-1,4,5,8-bis-(dicarboximide)-2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)}, and a high-*k* polymer gate dielectric, poly(vinylidene fluoride–trifluoroethylene–chlorofluoroethylene) ($k \approx 60$), are successfully fabricated on flexible substrates. A thin layer of Au nanoparticles is embedded in the gate dielectric, which can store injected charge from the channel and result in a memory effect. The organic memories demonstrate high carrier mobilities (>0.3 $cm^2/(V\ s)$), low program/erase voltages (±6 V), little degradation after 10^5 program/erase cycles, and good retention after 10^5 s, which suggest great promise in the application of nonvolatile memories in flexible electronics.



KEYWORDS: *floating-gate memory, high-k polymer, organic thin-film transistor, solution-processable, flexible*

INTRODUCTION

In the past two decades, great progress has been made in organic electronics for various important applications, including organic light-emitting diodes,[1] organic solar cells,[2−4] sensors,[5−7] and organic thin-film transistors (OTFTs).[8−12] The development of organic integrated circuits necessitates the fabrication of compatible organic memories as regular components.[13] Various organic memory devices, including polymer ferroelectric,[14] resistive,[15] electret,[16] and flash[17−26] memories, have been extensively studied. It is worth noting that flash memories based on organic floating-gate field-effect transistors (OFGTs) have been considered as the most promising candidates due to the nondestructive readout and the feasibility of integrating memories directly in transistor-based circuits, which is similar to the Si-based counterparts commercially used in the market.[17]

The majority of the reported OFGTs were fabricated with p-type small-molecule organic semiconductors (e.g., pentacene) as the active layers, which were normally deposited by thermal evaporation.[17−21] Recently, OFGTs based on pentacene and self-assembled monolayers (SAMs) were successfully fabricated on flexible plastic substrates with an operational voltage of 6 V.[17,18] However, solution-processable OFGTs based on polymers have rarely been reported due to the difficulties in the fabrication of multilayer polymer thin films with ideal interfaces. Baeg et al.[22] reported solution-processed OFGTs based on semiconducting polymer poly[(9,9-dioctylfluorene-2,7-diyl)-*co*-bithiophene], polystyrene/cross-linked poly(4-vinylphenol) double-layer polymer dielectrics and Au nanoparticles embedded between the two dielectric layers for charge storage. Leung et al.[23] reported OFGTs with thiophene-based polymer semiconductors and polymer dielectrics. Polystyrene-*b*-poly(4-vinylpyridine) (PS-*b*-P4VP) and Cytop (CTL-809M, Asahi Glass) were used as the tunneling and controlling dielectrics in the devices, respectively. However, these devices have a relatively high operational voltage (≥20 V), which is the major problem for real applications, such as wearable electronics. It is notable that solution-processable low-voltage OFGTs have not been realized until now.

The only way to decrease the operational voltage of a transistor is to increase the gate capacitance C_i given by $C_i = \varepsilon_0 k/d$, where k and d are the relative dielectric constant and the thickness of the gate dielectric, respectively, and ε_0 is the dielectric permittivity of a vacuum. Therefore, high-*k* or ultrathin gate dielectrics could be used to achieve low operational voltages. There are clear limitations of coating ultrathin tunneling and controlling dielectrics by a solution process due to the generation of pinholes and the penetration of metal atoms from deposited electrodes.[27] Therefore, a feasible way to realize solution-processable low-voltage OFGTs is to use high-*k* polymer gate dielectrics, which can have both a high gate capacitance and low leakage. Recently, we reported

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that high-k relaxor ferroelectric polymer poly(vinylidene fluoride−trifluoroethylene−chlorofluoroethylene) (P(VDF−TrFE−CFE)) is an excellent gate dielectric for solution-processable low-voltage OTFTs.[28−30] The terpolymer P(VDF−TrFE−CFE) exhibits a high dielectric constant (~60), a high breakdown field, and low leakage.[28] The electrical properties of the relaxor ferroelectric polymers are completely different from those of the ferroelectric polymers. Relaxor ferroelectric polymer capacitors show very little hysteresis (see the Supporting Information, Figure S1). Therefore, they are also a suitable gate dielectric material for OFGTs that has never been reported before. Although the terpolymer P(VDF−TrFE−CFE) was also used in ferroelectric memories recently,[31] application as the gate dielectric in OFGTs has completely different requirements and working mechanisms.

In this paper, we report low-voltage OFGTs prepared by a solution process for the first time. High-mobility n-type semiconducting polymer poly{[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2)) was used as the active layer.[11] It is notable that only a few n-type organic semiconductors have been successfully used in OFGTs.[20,23] To decrease the operational voltage of the devices, we used high-k polymer dielectrics as gate insulators, where poly(vinyl alcohol) (PVA; k = 7.9)[32] and P(VDF−TrFE−CFE) (k = 60)[28] were used as tunneling and controlling dielectrics, respectively. Pure PVA polymer does not have any charge-trapping effect and has a relatively high dielectric constant.[33] Therefore, it was chosen as the tunneling dielectric in our devices. A thin layer of Au nanoparticles was coated between the PVA and P(VDF−TrFE−CFE) layers for charge storage. The devices demonstrated an operational voltage of ±6 V, good retention longer than 10^5 s, excellent endurance properties for more than 10^5 program/erase cycles, and high carrier mobilities (>0.3 cm^2/(V s)).

EXPERIMENTAL SECTION

Materials. P(NDI2OD-T2) (N2200) was purchased from Polyera Corp. (United States) without further purification. PVA (M_n = 146−186 kg mol^{-1}) was purchased from Sigma-Aldrich. P(VDF−TrFE−CFE) (56 mol %/36.5 mol %/7.5 mol %) terpolymer was synthesized by the suspension polymerization process.[28,34]

Device Fabrication. The architecture of the floating-gate memories based on a top-gate bottom-contact transistor is shown in Figure 1a. It is notable that the two dielectrics PVA and P(VDF−TrFE−CFE) have orthogonal solvents, which is important for the preparation of multilayer films by a solution process. Au films (30 nm thick) were thermally evaporated on the surface of poly(ethylene terephthalate) (PET) substrates as source and drain electrodes through a shadow mask. The channel length (L) and width (W) were 100 μm and 2 mm, respectively. Conjugated polymer P(NDI2OD-T2) was dissolved in toluene at a concentration of 5 mg/mL and heated to 80 °C. The solution of P(NDI2OD-T2) polymer was spin-coated on the PET substrates with Au source/drain electrodes and annealed at 120 °C for 1 h in a glovebox filled with high-purity nitrogen. PVA polymer was dissolved in deionized (DI) water with a concentration of 6 mg/mL and spin-coated on P(NDI2OD-T2) to form the tunneling insulator layer followed by thermal annealing at 60 °C for 3 h to evaporate the DI water. Au nanoparticles acting as the floating gate were deposited by thermal evaporation and monitored by a quartz crystal thickness monitor. The high-k terpolymer P(VDF−TrFE−CFE) (56 mol %/36.5 mol %/7.5 mol %) was dissolved in methyl ethyl ketone at a concentration of 30 mg/mL and spin-coated on the Au nanoparticles. The P(VDF−TrFE−CFE) films were annealed at 60 °C for 3 h to evaporate the solvent. Finally, 100 nm thick Al gate electrodes were evaporated on the P(VDF−TrFE−CFE) films through a shadow mask.

Device Characterization. The OTFTs and OFGT-based memories were characterized with a semiconductor parameter analyzer (Agilent 4156C) in a glovebox. The field effect mobility of each transistor was calculated in the saturation region ($|V_D| \geq |V_G|$) by plotting the square root of the drain current versus the gate voltage and is given by the following equation:

$$\mu = \frac{2L}{WC_i}\left(\frac{d\sqrt{I_{DS}}}{dV_G}\right)^2 \quad (1)$$

where C_i is the capacitance of the gate insulator per unit area and W and L are the channel width and length of the device. For the bilayer gate dielectric

$$C_i = \frac{\varepsilon_0}{d_1/k_1 + d_2/k_2} \quad (2)$$

where d_1 and d_2 are the thicknesses of dielectric layers 1 and 2, respectively, and k_1 and k_2 are the relative dielectric constants of layers 1 and 2, respectively.

The surface morphology and the thicknesses of the polymer thin films were characterized by atomic force microscopy (AFM) (Veeco Instruments Inc.). Au nanoparticles on PVA films were observed under transmission electron microscopy (TEM; F2010, Japan).

RESULTS AND DISCUSSION

Figure 1a shows a schematic diagram of an OFGT with a top-gate and bottom-contact structure fabricated on a 150 μm thick flexible PET substrate. The thicknesses of the PVA and P(VDF−TrFE−CFE) layers are about 20 and 160 nm, respectively. Figure 1b shows a photograph of the flexible devices. A thin layer of Au nanoparticles with an average

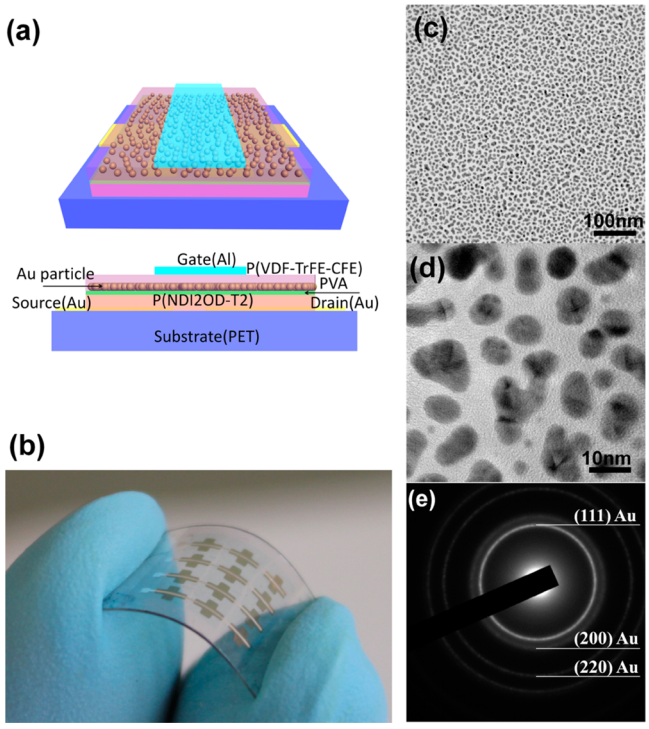

Figure 1. (a) Schematic diagram of a polymer floating-gate field-effect transistor with a top-gate bottom-contact structure. (b) Photograph of OFGTs on a flexible PET substrate. (c, d) TEM images of Au nanoparticles on a PVA film. (e) Electron diffraction pattern of Au nanoparticles under TEM.

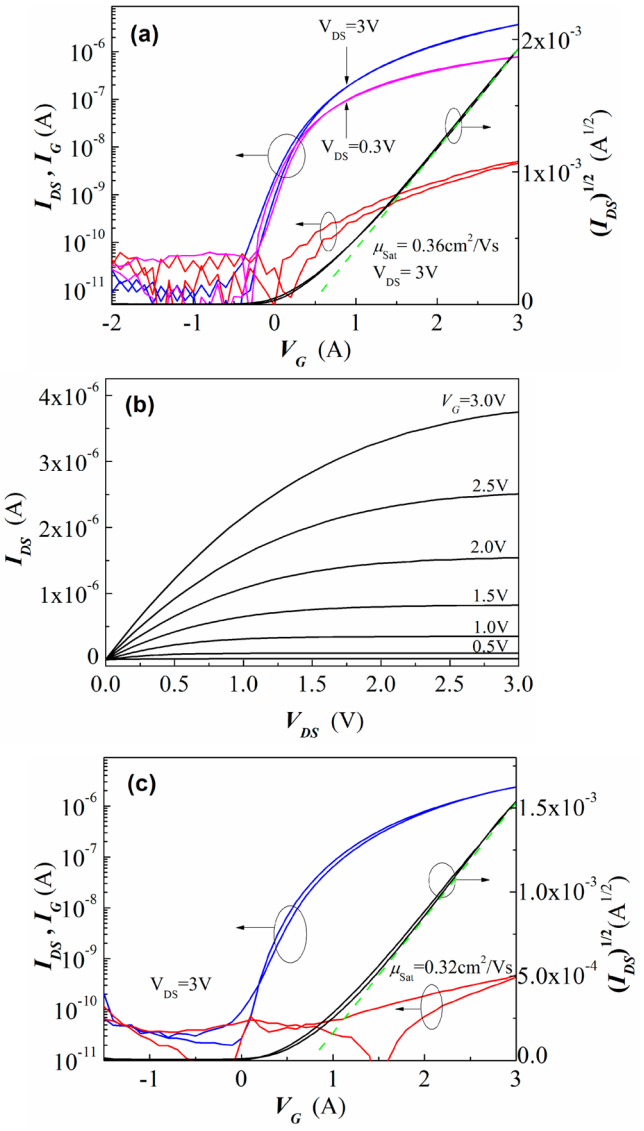

Figure 2. (a) Transfer ($I_{DS} \approx V_G$) and (b) output ($I_{DS} \approx V_{DS}$) characteristics of an OFGT measured below 3 V. (c) Transfer characteristics of an OTFT (control device) with a PVA/P(VDF−TrFE−CFE) double-layer gate dielectric.

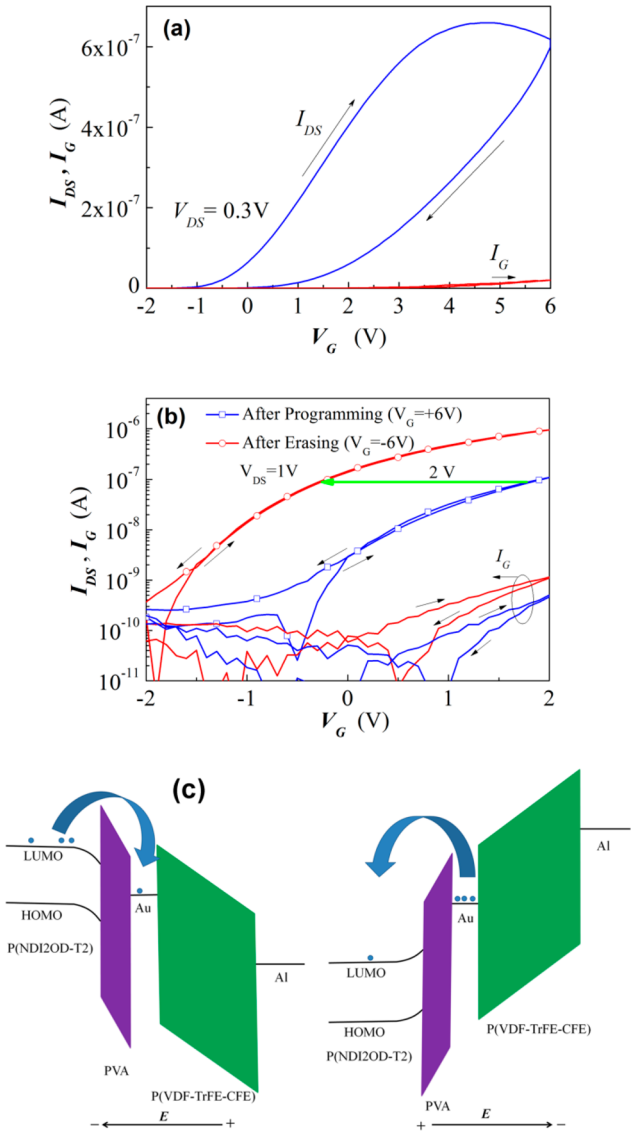

Figure 3. (a) Transfer characteristics of an OFGT measured at gate voltages between −2 and +6 V. (b) Transfer characteristics of the OFGT measured after programming at V_G = 6 V and after erasing at V_G = −6 V. (c) Energy band diagrams of an OFGT under positive (left) and negative (right) gate voltages.

thickness of ∼3 nm as a charge-trapping layer was deposited on a PVA film by thermal evaporation prior to the coating of a P(VDF−TrFE−CFE) layer.[22] Figure 1c shows a transmission electron microscopy image of the uniformly distributed Au nanoparticles on a PVA film. The average number of Au nanoparticles per unit area is estimated to be 6.7 × 10^{11} nanoparticles/cm^2. The high-resolution TEM image in Figure 1d clearly indicates particles with a size of about 5−10 nm. Figure 1e shows the selected area electron diffraction pattern of the Au nanoparticles. It is notable that the particle size can be controlled by the duration of thermal evaporation.[22] Compared to a continuous floating gate, Au nanoparticles are independent charge-storage sites isolated from each other, which will be more robust against loss of charge.

Parts a and b of Figure 2 show the transfer and output characteristics of an OFGT at an operational voltage of 3 V, respectively. The *n*-channel device has an electron mobility of 0.36 cm^2/(V s) and an on/off ratio of 10^5, which are comparable to those of the OTFTs based on P(NDI2OD-T2) at an operational voltage of 60 V reported by Yan et al.[11] More importantly, the device shows little hysteresis in the transfer curve when the gate voltage is below 3 V, indicating that the P(NDI2OD-T2)/PVA interface is very stable and charge injection from P(NDI2OD-T2) to Au nanoparticles does not occur at low gate voltages. The devices showed very stable performance after being kept for a long time (16 months) and after 100 bending tests with a radius of 9 mm (see the Supporting Information, Figures S2 and S3). To investigate the influence of the Au nanoparticles on the performances of the OFGTs, control OTFTs with the double-layer gate dielectric PVA/P(VDF−TrFE−CFE) without Au nanoparticles were fabricated at the same conditions. As shown in Figure 2 c, the carrier mobility, threshold voltage, and on/off ratio of a control device at an operational voltage of 3 V are 0.32 cm^2/(V s), 0.32 V, and 10^5, respectively, which are similar to those of the OFGT with Au nanoparticles. If the Au nanoparticles penetrated through the PVA layer to the semiconductor layer,

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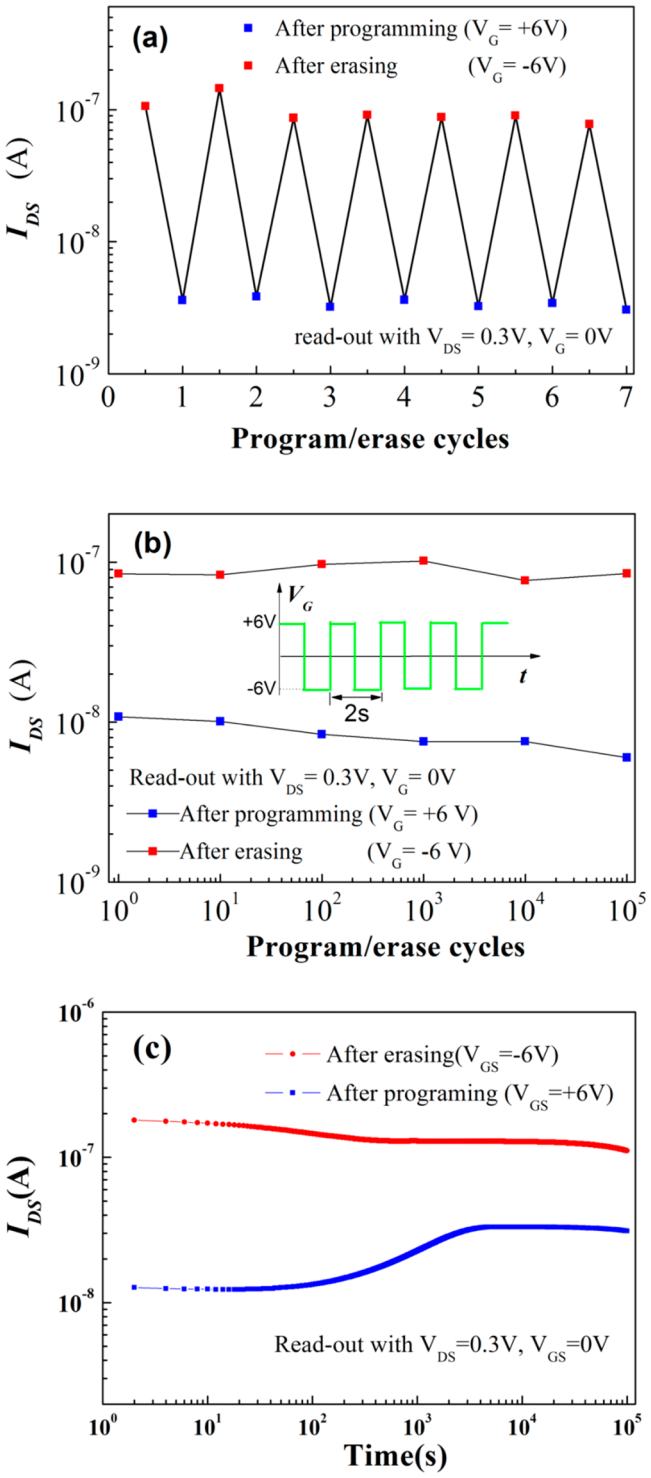

Figure 4. Channel currents of the OFGT measured at V_G = 0 V and V_{DS} = 0.3 V after programming and erasing (a) 7 times and (b) 10^5 times. (c) Time-dependent channel currents of an OFGT after programming or erasing.

the interface between the semiconductor and the PVA dielectric would be contaminated and the carrier mobilities of the devices would be decreased.[22] Therefore, the deposition of Au nanoparticles did not change the semiconductor/dielectric interface and had little effect on the performance of the OFGTs at gate voltages lower than 3 V.

It is notable that the OFGTs show a memory effect at higher gate voltages. Figure 3a shows the transfer characteristics of the device measured at gate voltages between −2 and +6 V. A big hysteresis between the forward and backward sweeps can be observed. It is notable that, in our control device without Au nanoparticles, the transfer curve showed a little hysteresis (see the Supporting Information, Figure S4). For the devices with Au nanoparticles, electron injection from the channel to the Au nanoparticles occurs at gate voltages higher than 3 V. The electrons stored in the Au floating gate induce a shift of the threshold voltage of the device to a more positive value. More importantly, we find that the threshold voltage can be recovered to its original value when −6 V is applied on the gate, indicating that the electrons in the Au nanoparticles can be removed by applying a high negative gate voltage. Therefore, the programmable memory behavior of the OFGT can be realized, which is attributed to charging/discharging of the Au nanoparticles during the program/erase operations.

Next, the memory properties of the OFGT were tested. During the program (erase) operations, V_G = +6 V (−6 V) and V_{DS} = 0 V were applied on the device for 1 s. To read the stored information in the device, we measured the transfer curve at low gate voltages that would not induce additional charge injection. The readout operations were performed with the gate voltage V_G swept between −2 and +2 V and V_{DS} = 1 V. Figure 3b shows the transfer characteristics of the two readout operations, which exhibit a sufficiently large memory window of about 2 V. The different channel currents due to the shift of the transfer curve can be defined as two states (on and off) of the memory. In addition, Figure 3 b shows that the gate leakage currents of the device are lower than 1.1 nA, implying a good insulating property of the gate dielectric that is critical to the retention property of the memory after program/erase operations.

Figure 3 c shows the energy band diagram of an OFGT under different gate voltages. When a high positive voltage is applied to the top-gate electrode (program operation, left device), electrons are injected into the Au nanoparticles from the P(NDI2OD-T2) layer through the 20 nm thick PVA tunneling layer due to tunneling or a thermal emission process driven by the applied electric field.[18,20,35] Fowler−Nordheim tunneling mechanics has been proposed to explain the charge tunneling in OFGTs by M. Kaltenbrunner et al.[18] and K. Baeg et al.[22] Due to the similar device structure, the charge injection in our OFGT can also be attributed to the Fowler−Nordheim tunneling process.[18] In the readout operation, the threshold voltage (V_{th}) is shifted to a more positive value because the gate bias is screened by the stored electrons in the Au nanoparticles. On the other hand, when a high negative voltage is applied on the top-gate electrode, the stored electrons in the Au nanoparticles are injected back into the P(NDI2OD-T2) layer, as shown in Figure 3c (erase operation, right device). Therefore, V_{th} is shifted to a more negative voltage in the readout operation. The trapped charge carrier density in the Au nanoparticles can be calculated by using the equation $Q = C_{ci}\Delta V_{th}$, where C_{ci} = 375 nF/cm^2 is the capacitance per unit area of the P(VDF−TrFE−CFE) controlling layer of the gate dielectric and ΔV_{th} is the memory window. Therefore, the stored electron density in the floating gate is estimated to be about 4.7 × 10^{12}/cm^2, which means that about 7 electrons on average are trapped in each Au nanoparticle.

Nonvolatile memory devices should have good charge retention and cycling endurance capabilities. The channel

currents were measured at V_G = 0 V and V_{DS} = 0.3 V as a function of the number of program/erase cycles to demonstrate the difference between on/off states. Figure 4a shows the results after several program/erase cycles, which exhibit the channel current difference between on and off states for about 1 order of magnitude. To achieve more program/erase cycles, a continuous square signal with voltages of ±6 V and a period of 2 s, as shown in the inset of Figure 4b, was applied between the gate and the source/drain electrodes to test the cycling endurance. The channel currents corresponding to the on/off states after a different number of cycles are shown in Figure 4b. It is notable that almost no degradation in the channel currents can be observed after 10^5 program/erase cycles, which is comparable to that of the commercially used silicon-based flash memories.[36] Therefore, the cycling endurance capability is much better than that of most of the reported organic floating-gate memories.[17−24] In fact, up to 10^4 endurance cycles in a conventional Si-based nonvolatile memory is enough for practice applications.[36]

The time-dependent channel currents at V_G = 0 V and V_{DS} = 0.3 V after program/erase operations were characterized to exhibit the charge retention property of the OFGT memory, as shown in Figure 4c. It is notable that the channel currents after programming increase with time and the ratio between on and off currents decreases from 14 to 3 after 10^5 s. The degradation is due to the leakage current between the Au floating gate and the active layer, which can be optimized by increasing the thickness of the PVA tunneling layer. However, a thicker PVA layer will induce a higher operational voltage. We found that a 20 nm thick PVA layer showed the broadest memory window at an operational voltage of 6 V (see the Supporting Information, Figure S5), which is the optimized thickness of PVA in our devices. Therefore, the ideal thickness of the PVA layer is a compromise between a good retention property and a low operational voltage. Nevertheless, the retention property of the OFGT is comparable to that of the reported OFGTs based on pentacene.[17]

CONCLUSIONS

In summary, we have successfully fabricated low-voltage nonvolatile floating-gate memories on flexible substrates by a solution process for the first time. The devices are based on high-mobility n-type semiconducting polymer P(NDI2OD-T2) and high-*k* polymer gate dielectrics P(VDF−TrFE−CFE) and PVA. The organic memories demonstrate a high carrier mobility (>0.3 $cm^2/(V\ s)$), low program/erase voltages (±6 V), an excellent endurance capability after 10^5 program/erase cycles, and a good retention property after 10^5 s, which suggest promising applications in flexible electronics as nonvolatile memories.

ASSOCIATED CONTENT

Supporting Information

Figures showing the polarization-voltage loop of the Al/(160 nm)P(VDF-TrFE-CFE)/Al capacitor device, transfer curves of an OFGT characterized before and after 16 months and an OFGT characterized before and after 100 bending tests, transfer curve of the control device without Au nanoparticles, and transfer characteristics of OFGTs with different PVA thicknesses. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Burroughes, J. H.; Bradley, D. D. C.; Brown, A. R.; Marks, R. N.; Mackay, K.; Friend, R. H.; Burns, P. L.; Holmes, A. B. Light-Emitting Diodes Based on Conjugated Polymers. *Nature* **1990**, *347*, 539−541.

(2) Li, G.; Shrotriya, V.; Huang, J.; Yao, Y.; Moriarty, T.; Emery, K.; Yang, Y. High-Efficiency Solution Processable Polymer Photovoltaic Cells by Self-Organization of Polymer Blends. *Nat. Mater.* **2005**, *4*, 864−868.

(3) Liu, Z.; Li, J.; Yan, F. Package-Free Flexible Organic Solar Cells with Graphene Top Electrodes. *Adv. Mater.* **2013**, *25*, 4296−4301.

(4) Tai, Q.; Li, J.; Liu, Z.; Sun, Z.; Zhao, X.; Yan, F. Enhanced Photovoltaic Performance of Polymer Solar Cells by Adding Fullerene End-Capped Polyethylene Glycol. *J. Mater. Chem.* **2011**, *21*, 6848−6853.

(5) Sun, Z.; Li, J.; Liu, C.; Yang, S.; Yan, F. Enhancement of Hole Mobility of Poly(3-hexylthiophene) Induced by Titania Nanorods in Composite Films. *Adv. Mater.* **2011**, *23*, 3648−3652.

(6) Lin, P.; Yan, F. Organic Thin-Film Transistors for Chemical and Biological Sensing. *Adv. Mater.* **2012**, *24*, 34−51.

(7) Lin, P.; Yan, F.; Yu, J.; Chan, H. L. W.; Yang, M. The Application of Organic Electrochemical Transistors in Cell-Based Biosensors. *Adv. Mater.* **2010**, *22*, 3655−3660.

(8) Sirringhaus, H.; Tessler, N.; Friend, R. H. Integrated Optoelectronic Devices Based on Conjugated Polymers. *Science* **1998**, *280*, 1741−1744.

(9) Halik, M.; Klauk, H.; Zschieschang, U.; Schmid, G.; Dehm, C.; Schutz, M.; Maisch, S.; Effenberger, F.; Brunnbauer, M.; Stellacci, F. Low-Voltage Organic Transistors with an Amorphous Molecular Gate Dielectric. *Nature* **2004**, *431*, 963−966.

(10) McCulloch, I.; Heeney, M.; Bailey, C.; Genevicius, K.; MacDonald, I.; Shkunov, M.; Sparrowe, D.; Tierney, S.; Wagner, R.; Zhang, W.; Chabinyc, M. L.; Kline, R. J.; McGehee, M. D.; Toney, M. F. Liquid-Crystalline Semiconducting Polymers with High Charge-Carrier Mobility. *Nat. Mater.* **2006**, *5*, 328−333.

(11) Yan, H.; Chen, Z.; Zheng, Y.; Newman, C.; Quinn, J. R.; Dotz, F.; Kastler, M.; Facchetti, A. A High-Mobility Electron-Transporting Polymer for Printed Transistors. *Nature* **2009**, *457*, 679−686.

(12) Tang, W.; Feng, L.; Zhao, J.; Cui, Q.; Chen, S.; Guo, X. Inkjet Printed Fine Silver Electrodes for All-Solution-Processed Low-Voltage Organic Thin Film Transistors. *J. Mater. Chem. C* **2014**, *2*, 1995−2000.

(13) Ren, X. C.; Wang, S. M.; Leung, C. W.; Yan, F.; Chan, P. K. L. Thermal Annealing and Temperature Dependences of Memory Effect in Organic Memory Transistor. *Appl. Phys. Lett.* **2011**, *99*, 043303.

(14) Naber, R. C. G.; Tanase, C.; Blom, P. W. M.; Gelinck, G. H.; Marsman, A. W.; Touwslager, F. J.; Setayesh, S.; de Leeuw, D. M. High-Performance Solution-Processed Polymer Ferroelectric Field-Effect Transistors. *Nat. Mater.* **2005**, *4*, 243−248.

(15) Son, D. I.; Kim, T. W.; Shim, J. H.; Jung, J. H.; Lee, D. U.; Lee, J. M.; Park, W. I.; Choi, W. K. Flexible Organic Bistable Devices Based on Graphene Embedded in an Insulating Poly(methyl methacrylate) Polymer Layer. *Nano Lett.* **2010**, *10*, 2441−2447.

(16) Baeg, K. J.; Noh, Y. Y.; Ghim, J.; Kang, S. J.; Lee, H.; Kim, D. Y. Organic Non-Volatile Memory Based on Pentacene Field-Effect

Transistors Using a Polymeric Gate Electret. *Adv. Mater.* **2006**, *18*, 3179−3183.
(17) Sekitani, T.; Yokota, T.; Zschieschang, U.; Klauk, H.; Bauer, S.; Takeuchi, K.; Takamiya, M.; Sakurai, T.; Someya, T. Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays. *Science* **2009**, *326*, 1516−1519.
(18) Kaltenbrunner, M.; Stadler, P.; Schwödiauer, R.; Hassel, A. W.; Sariciftci, N. S.; Bauer, S. Anodized Aluminum Oxide Thin Films for Room-Temperature-Processed, Flexible, Low-Voltage Organic Non-Volatile Memory Elements with Excellent Charge Retention. *Adv. Mater.* **2011**, *23*, 4892−4896.
(19) Kim, S.-J.; Lee, J.-S. Flexible Organic Transistor Memory Devices. *Nano Lett.* **2010**, *10*, 2884−2890.
(20) Leong, W. L.; Mathews, N.; Tan, B.; Vaidyanathan, S.; Dotz, F.; Mhaisalkar, S. Towards Printable Organic Thin Film Transistor Based Flash Memory Devices. *J. Mater. Chem.* **2011**, *21*, 5203−5214.
(21) Heremans, P.; Gelinck, G. H.; Müller, R.; Baeg, K.-J.; Kim, D.-Y.; Noh, Y.-Y. Polymer and Organic Nonvolatile Memory Devices. *Chem. Mater.* **2010**, *23*, 341−358.
(22) Baeg, K.-J.; Noh, Y.-Y.; Sirringhaus, H.; Kim, D.-Y. Controllable Shifts in Threshold Voltage of Top-Gate Polymer Field-Effect Transistors for Applications in Organic Nano Floating Gate Memory. *Adv. Funct. Mater.* **2010**, *20*, 224−230.
(23) Leong, W. L.; Mathews, N.; Tan, B.; Vaidyanathan, S.; Dotz, F.; Mhaisalkar, S. Solution Processed Non-Volatile Top-Gate Polymer Field-Effect Transistors. *J. Mater. Chem.* **2011**, *21*, 8971−8974.
(24) Wei, Q.; Lin, Y.; Anderson, E. R.; Briseno, A. L.; Gido, S. P.; Watkins, J. J. Additive-Driven Assembly of Block Copolymer−Nanoparticle Hybrid Materials for Solution Processable Floating Gate Memory. *ACS Nano* **2012**, *6*, 1188−1194.
(25) Han, S.-T.; Zhou, Y.; Roy, V. A. L. Towards the Development of Flexible Non-Volatile Memories. *Adv. Mater.* **2013**, *25*, 5425−5449.
(26) Han, S.-T.; Zhou, Y.; Wang, C.; He, L.; Zhang, W.; Roy, V. A. L. Layer-by-Layer-Assembled Reduced Graphene Oxide/Gold Nanoparticle Hybrid Double-Floating-Gate Structure for Low-Voltage Flexible Flash Memory. *Adv. Mater.* **2013**, *25*, 872−877.
(27) Chua, L.-L.; Ho, P. K. H.; Sirringhaus, H.; Friend, R. H. High-Stability Ultrathin Spin-On Benzocyclobutene Gate Dielectric for Polymer Field-Effect Transistors. *Appl. Phys. Lett.* **2004**, *84*, 3400−3402.
(28) Li, J.; Sun, Z.; Yan, F. Solution Processable Low-Voltage Organic Thin Film Transistors with High-*k* Relaxor Ferroelectric Polymer as Gate Insulator. *Adv. Mater.* **2012**, *24*, 88−93.
(29) Li, J.; Liu, D.; Miao, Q.; Yan, F. The Application of a High-*k* Polymer in Flexible Low-Voltage Organic Thin-Film Transistors. *J. Mater. Chem.* **2012**, *22*, 15998−16004.
(30) Pattanasattayavong, P.; Yaacobi-Gross, N.; Zhao, K.; Ndjawa, G. O. N.; Li, J.; Yan, F.; O'Regan, B. C.; Amassian, A.; Anthopoulos, T. D. Hole-Transporting Transistors and Circuits Based on the Transparent Inorganic Semiconductor Copper(I) Thiocyanate (CuSCN) Processed from Solution at Room Temperature. *Adv. Mater.* **2013**, *25*, 1504−1509.
(31) Hwang, S. K.; Bae, I.; Cho, S. M.; Kim, R. H.; Jung, H. J.; Park, C. High Performance Multi-Level Non-Volatile Polymer Memory with Solution-Blended Ferroelectric Polymer/High-*k* Insulators for Low Voltage Operation. *Adv. Funct. Mater.* **2013**, *23*, 5484−5493.
(32) Li, J.; Du, J.; Xu, J.; Chan, H. L. W.; Yan, F. The Influence of Gate Dielectrics on a High-Mobility n-Type Conjugated Polymer in Organic Thin-Film Transistors. *Appl. Phys. Lett.* **2012**, *100*, 033301−033304.
(33) Egginger, M.; Irimia-Vladu, M.; Schwödiauer, R.; Tanda, A.; Frischauf, I.; Bauer, S.; Sariciftci, N. S. Mobile Ionic Impurities in Poly(vinyl alcohol) Gate Dielectric: Possible Source of the Hysteresis in Organic Field-Effect Transistors. *Adv. Mater.* **2008**, *20*, 1018−1022.
(34) Chung, T. C.; Petchsuk, A. Synthesis and Properties of Ferroelectric Fluoroterpolymers with Curie Transition at Ambient Temperature. *Macromolecules* **2002**, *35*, 7678−7684.
(35) Yan, F.; Hong, Y.; Chan, H. L. W. Measurement of Ultralow Injection Current to Polymethyl-Methacrylate Film. *Appl. Phys. Lett.* **2008**, *92*, 243301.
(36) Bez, R.; Camerlenghi, E.; Modelli, A.; Visconti, A. Introduction to Flash Memory. *Proc. IEEE* **2003**, 489−502.